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Devadas, S.; Newton, A.R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 10, Issue 1, Jan. 1991 Page(s):13 - 27
Digital Object Identifier 10.1109/43.62788

AbstractPlus | Full Text: PDF(1476 KB)   IEEE JNL

☐   2. **Local search for satisfiability (SAT) problem**
Gu, J.;
Systems, Man and Cybernetics, IEEE Transactions on
Volume 23, Issue 4, July-Aug. 1993 Page(s):1108 - 1129
Digital Object Identifier 10.1109/21.247892

AbstractPlus | Full Text: PDF(1752 KB)   IEEE JNL

☐   3. **Test generation for cyclic combinational circuits**
Raghunathan, A.; Ashar, P.; Malik, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 14, Issue 11, Nov. 1995 Page(s):1408 - 1414
Digital Object Identifier 10.1109/43.469666

AbstractPlus | Full Text: PDF(636 KB)   IEEE JNL

☐   4. **Hazard-free implementation of speed-independent circuits**
Kondratyev, A.; Kishinevsky, M.; Yakovlev, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
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AbstractPlus | References | Full Text: PDF(600 KB)   IEEE JNL

☐   5. **IGRAINE-an Implication GRaph-bAsed engINE for fast implication, justific propagation**
Tafertshofer, P.; Ganz, A.; Antreich, K.J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 19, Issue 8, Aug. 2000 Page(s):907 - 927
Digital Object Identifier 10.1109/43.856977

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Cordone, R.; Ferrandi, F.; Sciuto, D.; Calvo, R.W.;
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Blank, C.; Eveking, H.; Levihn, J.; Ritter, G.;
High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IE
7-9 Nov. 2001 Page(s):45 - 50
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Peixin Zhong; Ashar, P.; Malik, S.; Martonosi, M.;
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15-19 Jun 1998 Page(s):194 - 199

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Evolutionary Computation, 1997., IEEE International Conference on
13-16 April 1997 Page(s):43 - 48
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Murgai, R.; Fujita, M.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):232 - 238
Digital Object Identifier 10.1109/ICVD.1997.568081

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☐ 1. **Path sensitization in critical path problem [logic circuit design]**
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Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
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Liu, L.-R.; Chen, H.-C.; Du, D.H.C.;
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Chanhee Oh; Mercer, M.R.;
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Industrial Electronics, IEEE Transactions on
Volume 36, Issue 2, May 1989 Page(s):117 - 128
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AbstractPlus | Full Text: PDF(980 KB)   IEEE JNL

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AbstractPlus | References | Full Text: PDF(228 KB)   IEEE JNL

☐   **25. Functional vector generation for HDL models using linear programming ;**
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1 Non-Enumerative Path Delay Fault Diagnosis   ■
Saravanan Padmanaban, Spyros Tragoudas
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society
Full text available: 📄 pdf(211.24 KB)   Additional Information: full citation, abstract, index terms
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The first non-enumerative framework for diagnosing path delay faults using zero suppressed binary decision diagrams is introduced. We show that fault free path delay faults with a validated non-robust test may together with fault free robustly tested faults be used to eliminate faults from the set of suspected faults. All operations are implemented by an implicit diagnosis tool based on the zero suppressed binary decision diagram. The proposed method is space and time non-enumerative as opposed ...

2 Analysis of cyclic combinational circuits   ■
Sharad Malik
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society Press
Full text available: 📄 pdf(770.89 KB)   Additional Information: full citation, references, citings

3 Session S3.1: architecture adaptation and synthesis: Cycle-time aware architecture   ■
◈ synthesis of custom hardware accelerators
Mukund Sivaraman, Shail Aditya
October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**
Publisher: ACM Press
Full text available: 📄 pdf(75.23 KB)   Additional Information: full citation, abstract, references, index terms

We present the cycle-time aware architecture synthesis methodology used in PICO-NPA that automatically synthesizes minimal cost RT-level designs from high-level specifications to meet a given cycle-time. This allows subsequent physical synthesis to succeed on first pass with predictable performance. The core of the methodology is a static timing analysis engine that is used at multiple levels - program-level, architecture-level and RT-level - in order to identify, schedule and validate useful op ...

Keywords: clock frequency, delay analysis, embedded hardware architecture synthesis, high-level synthesis, operator chaining, target clock period, timing analysis, timing during scheduling

4 Oscillation control in logic simulation using dynamic dominance graphs ■

Peter Dahlgren

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available: 📄 pdf(125.57 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

5 Desensitization for power reduction in sequential circuits ■

Xiangfeng Chen, Peicheng Pen, C. L. Liu

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available: 📄 pdf(183.09 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

6 Tutorial: Compiling concurrent languages for sequential processors ■

Stephen A. Edwards

April 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 8 Issue 2

Publisher: ACM Press

Full text available: 📄 pdf(771.65 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>, <u>review</u>

Embedded systems often include a traditional processor capable of executing sequential code, but both control and data-dominated tasks are often more naturally expressed using one of the many domain-specific concurrent specification languages. This article surveys a variety of techniques for translating these concurrent specifications into sequential code. The techniques address compiling a wide variety of languages, ranging from dataflow to Petri nets. Each uses a different method, to some degr ...

Keywords: Compilation, Esterel, Lustre, Petri nets, Verilog, code generation, communication, concurrency, dataflow, discrete-event, partial evaluation, sequential

7 Automated multi-cycle symbolic timing verification of microprocessor-based designs ■

Anurag P. Gupta, Daniel P. Siewiorek

June 1994 **Proceedings of the 31st annual conference on Design automation**

Publisher: ACM Press

Full text available: 📄 pdf(140.84 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

8 Functional vector generation for HDL models using linear programming and 3-satisfiability ■

Farzan Fallah, Srinivas Devadas, Kurt Keutzer

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: 📄 pdf(252.59 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>
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Our strategy for automatic generation of functional vectors is based on exercising selected paths in the given hardware description language (HDL) model. The HDL model describes interconnections of arithmetic, logic and memory modules. Given a path in the HDL model, the search for input stimuli that exercise the path can be converted into a standard satisfiability checking problem by expanding the arithmetic modules into logic-gates. However, this approach is not very efficient. ...

Keywords: MPEG4, codec, design automatian, flip-flops, level converters, low power, placement, synthesis, voltage scaling

9 <u>Digital test generation and design for testability</u>

John Grason, Andrew W. Nagle
June 1980 **Proceedings of the 17th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(1.42 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

This paper is a tutorial intended primarily for individuals just getting started in digital testing. Basic concepts of testing are described, and the steps in the test development process are discussed. A pragmatic approach to test sequence generation is presented, oriented towards ICs interconnected on a board. Finally, design for testability techniques are described, with an emphasis on solving problems that appeared during the test generation discussion.

10 <u>SAT based ATPG using fast justification and propagation in the implication graph</u>

Paul Tafertshofer, Andreas Ganz
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press

Full text available: pdf(179.42 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

In this paper we present new methods for fast justification and propagation in the implication graph (IG) which is the core data structure of our SAT based implication engine. As the IG model represents all information on the implemented logic function as well as the topology of a circuit, the proposed techniques inherit all advantages of both general SAT based and structure based approaches to justification, propagation, and implication. These three fundamental Boolean problems are ...

11 <u>Design methodologies for noise in digital integrated circuits</u>

Kenneth L. Shepard
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(222.60 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>
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In this paper, we describe the growing problems of noise in digital integrated circuits and the design tools and techniques used to ensure the noise immunity of digital designs.

Keywords: high-level synthesis, telecommunication

12 <u>Functional testing techniques for digital LSI/VLSI systems</u>

Stephen Y.H. Su, Tonysheng Lin
June 1984 **Proceedings of the 21st conference on Design automation**
Publisher: IEEE Press

Full text available: pdf(1.39 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Functional testing is becomilng more important due to the increasing complexity in digital LSI/VLSI devices. Various functional testing approaches have been proposed to meet this urgent need in LSI/VLSI testing. This paper presents the basic ideas behind deterministic functional testing and concisely overviews eight major functional testing techniques. Comparisons among these techniques and suggestions for future development are made to meet the challenges in this fast growing testing field ...

13 Power management techniques for control-flow intensive designs

Anand Raghunathan, Sujit Dey, Niraj K. Jha, Kazutoshi Wakabayashi

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Publisher: ACM Press

Full text available: pdf(187.17 KB)
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Additional Information: full citation, abstract, references, citings, index terms

This paper presents a low-overhead controller-based powermanagement technique that re-specifies control signals to reconfigureexisting multiplexer networks and functional units to minimizeunnecessary activity. We demonstrate that conventional powermanagement techniques may often not be suited to control-flowintensive designs, and provide a comprehensive analysis of thepotential negative effects of power management on circuit delay,glitching activity at control and data path signals, and formatio ...

14 Analyzing cycle stealing on synchronous circuits with level-sensitive latches

I. Lin, J. A. Ludwig, K. Eng

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(685.55 KB)

Additional Information: full citation, references, citings, index terms

15 Complexity of sequential ATPG

T. E. Marchok, A. El-Maleh, W. Maly, J. Rajski

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(1.20 MB)
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Additional Information: full citation, abstract, citings

The research reported in this paper was conducted to identify those attributes, of both sequential circuits and structural, sequential automatic test pattern generation (ATPG) algorithms, which can lead to extremely high test generation times. The retiming transformation is used as a mechanism to create two classes of circuits which present varying degrees of complexity for test generation. It was observed for three different sequential test generators that the increase in complexity of testing ...

Keywords: VLSI, automatic test pattern generation, automatic testing, circuit attribute, density of encoding, design for testability, integrated circuit testing, logic testing, retiming transformation, sequential ATPG, sequential circuits, structural ATPG, test generation times, testing complexity, timing

16 Path sensitization of combinational circuits and its impact on clocking of sequential systems

R. Peset Llopis

December 1995 **Proceedings of the conference on European design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(672.15 KB)   Additional Information: full citation, references, index terms

17 VIPER: an efficient vigorously sensitizable path extractor

Hoon Chang, Jacob A. Abraham

July 1993 **Proceedings of the 30th international conference on Design automation**

Publisher: ACM Press

Full text available: pdf(766.04 KB) Additional Information: full citation, references, citings, index terms

18 Provably correct high-level timing analysis without path sensitization

Subhrajit Bhattacharya, Sujit Dey, Franc Brglez

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(820.65 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the problem of true delay estimation during high level design. The existing delay estimation techniques either estimate the topological delay of the circuit which may be pessimistic, or use gate-level timing analysis for calculating the true delay, which may be prohibitively expensive.We show that the paths in the implementation of a behavioral specification can be partitioned into two sets, SP and UP. While the paths in SP can affect the delay of the circuit ...

19 Error-tolerant design: SEU tolerant device, circuit and processor design

William Heidergott

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(364.56 KB)   Additional Information: full citation, abstract, references, index terms

Development of highly reliable and available systems requires consideration of the occurrence of single event upsets, the effects they have on system performance, and strategies for their prevention and mitigation. Methods of systems engineering process and the application and validation of techniques for fault tolerance are discussed as elements in the elimination and mitigation of single event upsets.

Keywords: error detection and correction coding, fault avoidance, fault masking, fault tolerant systems, modular redundancy, radiation effects, single event upset, soft error rate, temporal redundancy

20 Incremental techniques for the identification of statically sensitizable critical paths

Yun-Cheng Ju, Resve A. Saleh

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Publisher: ACM Press

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L3	77	combinational near cycle$1	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:37
L4	795	feedback near cycle	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:37
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